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ATTORNEY DOCKET NO. 70030735-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Lee Kong Weng et al.

Serial No.: 10/669,986 Examiner: Sharon E. Payne

Filing Date: September 23, 2003 Group Art Unit: 2875

Title: Ceramic Packaging for High Brightness LED Devices

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF REPLY BRIEF

Sir:

Transmitted herewith is the Reply Brief in this application with respect to the Examiner's Answer mailed December 31, 2007.

The fee for filing this Reply Brief is (37 CFR 1.17(c)) $0.00

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
☐	four months	$1590.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 50-3718 the sum of $0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 50-3718 pursuant to 37 CFR 1.25.

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Respectfully submitted,

Lee Kong Weng et al.

By Thomas F. Woods

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Reg. No. 36,726

Date: Feb. 29, 2008

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Lee Kong Weng et al. Examiner: Name: Sharon E. Payne

Serial No.: 10/669,986 Group Art Unit: 2875

Filed: September 23, 2003 Attorney Docket No.: 70030735-1

Confirmation No.: 4231

Title: Ceramic Packaging for High Brightness LED Devices

REPLY BRIEF

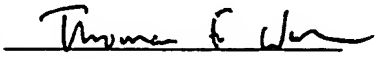
Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Arlington, VA 22313-1450

Sir:

In response to the Examiner's Answer mailed December 31, 2007, and further to the Final Office Action mailed July 6, 2007, 2007 and the Notice of Appeal filed September 7, 2007 in the present patent application, Applicants respectfully request entry of this Reply Brief, which pursuant to Section 1208 of the MPEP, 37 CFR 41.41 and 37 CFR 41.37(c) is intended to be a substitute brief, and allowance of the presently pending claims in the above-identified patent application.

DATE OF DEPOSIT: February 29, 2008

CERTIFICATE OF ELECTRONIC DEPOSIT: I hereby certify that all paper(s) described herein are being filed electronically with the United States Patent and Trademark Office Postal Service on the date indicated above and addressed to Mail Stop Appeal Brief - Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: 

Printed Name: Thomas F. Woods, Reg. No. 36,726

I. Real Party in Interest

The Real Party in Interest of the above-referenced patent application is Avago Technologies ECBU IP (Singapore) PTE., Ltd.

II. Related Appeals and Interferences

There are no related appeals or interferences respecting the above-referenced patent application.

III. Status of the Claims

Claims 1 and 3-14 remain pending in the present patent application and are hereby appealed herein. The status of each of the claims is as follows:

Claim 1: Rejected and appealed herein

Claim 2: Previously cancelled and *not* appealed herein

Claims 3-14: Rejected and appealed herein

Claims 15-19: Previously cancelled and *not* appealed herein

IV. Status of Amendments

Various amendments to the claims have been made and entered in the present application. Since the original filing date of the present patent application (September 23, 2003), no amendments have been requested or entered respecting the drawings or specification. Amendments to the claims are described in detail below.

In a Response and Amendment dated April 7, 2005, amendments to claims 1, 8 and 14 were requested by Applicants' attorney. In a Final Office Action dated June 22, 2005, the Examiner did not indicate explicitly that the amendments requested in the April 7 paper had been entered, but neither did she indicate they had not been entered. Comments and analyses made in June 22 Final Office Action were consistent, however, with such amendments having been entered.

In an Amendment and Response filed with a Request for Continuing Examination dated August 24, 2005, amendments to claims 1 and 14 were requested by Applicants' attorney. In a non-final Office Action dated October 4, 2005, the Examiner did not indicate explicitly that the amendments requested in the August 24 paper had been entered, but neither did she indicate they had not been entered. Comments and analyses made in October 4 Office Action were consistent, however, with such amendments having been entered.

In a Response and Amendment dated January 9, 2006, amendments to claim 8 were requested by Applicants' attorney. In a Final Office Action dated March 22, 2006, the Examiner did not indicate explicitly that the amendments requested in the January 9 paper had been entered, but neither did she indicate they had not been entered. Comments and analyses made

in March 22 Final Office Action were consistent, however, with such amendments having been entered.

In a Response to Non-Compliant Amendment dated October 24, 2006, amendments were requested to claims 1-3, 7-9 and 12-24. In a non-final Office Action dated January 22, 2007, the Examiner did not indicate explicitly that the amendments requested in the October 24 paper had been entered, but neither did she indicate they had not been entered. Comments and analyses made in January 22 Office Action were consistent, however, with such amendments having been entered.

In a Preliminary Amendment and Response filed in conjunction with an RCE dated April 23, 2007, amendments to claims 1, 8 and 13 were requested by Applicants' attorney. In a Final Office Action dated July 6, 2007, the Examiner did not indicate explicitly that the amendments requested in the April 23 paper had been entered, but neither did she indicate they had not been entered. Comments and analyses made in July 6 Final Office Action were consistent, however, with such amendments having been entered.

V. Summary of the Claimed Subject Matter

The invention set forth in the pending claims relates to an apparatus and a method associated with a standalone light emitting diode package comprising a housing having substantially vertical sidewalls and a substrate forming a single unitary piece of ceramic, a reflective coating disposed over at least portions of the sidewalls and the substrate, and an LED mounted in or on the substrate and covered by an optically transparent material, where the composition of the ceramic, configuration of the housing and the reflective coating cooperate to minimize light leakage through, into or out of the housing.

Unlike many prior art devices and methods, the package of the invention recited in the pending claims results in a small, thin, tough, electrically efficient LED lighting package that permits little or no light leakage therefrom or therethrough, except substantially along the azimuth in which light is intended to be directed. The low light leakage characteristics of the invention recited in the pending claims result in a lighting package that may be operated with lower power consumption and thus higher efficiency than lighting packages of the prior art. The invention recited in the pending claims also results in a lighting package that may also be made smaller and thinner than lighting packages of the prior art, and that may contain more LEDs than lighting packages of the prior art owing to the increased surface area, and thus increased heat-conducting capabilities, of the substantially vertical sidewalls.

Reference to claim 1 as amended herein is instructive, as it contains limitations similar to those found in all the other claims that yet remain pending in the present application. With further reference to Figs. 2D and 4

of the present application (also set forth hereinbelow), claim 1 recites the following:

(a) A standalone light emitting diode package, comprising:

(b) a housing comprising substantially vertical sidewalls and a substrate;

(c) the sidewalls and the substrate defining a cavity having a bottom, the substrate being located at the bottom of the cavity, the substrate and the vertical sidewalls being contiguous and continuous with one another at the intersections thereof;

(d) the housing forming a single unitary piece of ceramic;

(e) at least one light-reflective metallic coating disposed over at least portions of the sidewalls and the substrate;

(f) a light emitting diode mounted on or in the substrate, and

(g) an optically transparent material disposed in the cavity and covering the light emitting diode;

(h) wherein the ceramic composition and configuration of the housing and the light-reflective coating cooperate to minimize light leakage through, into or out of the housing when the light emitting diode is energized;

(i) the metallic coating reflects light incident thereon in a predetermined direction, and

(j) the optically transparent material protects the light emitting diode.

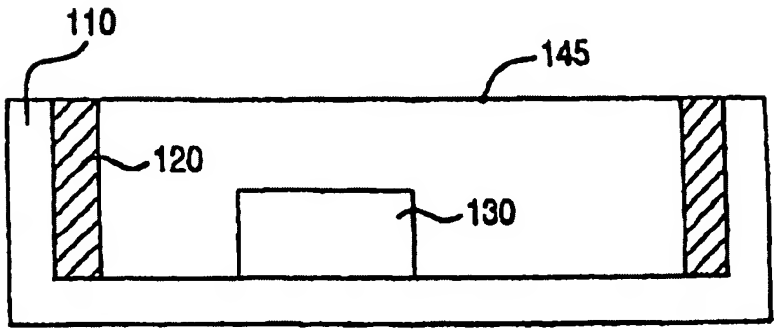


Figure 2D

Fig. 2D of the present application

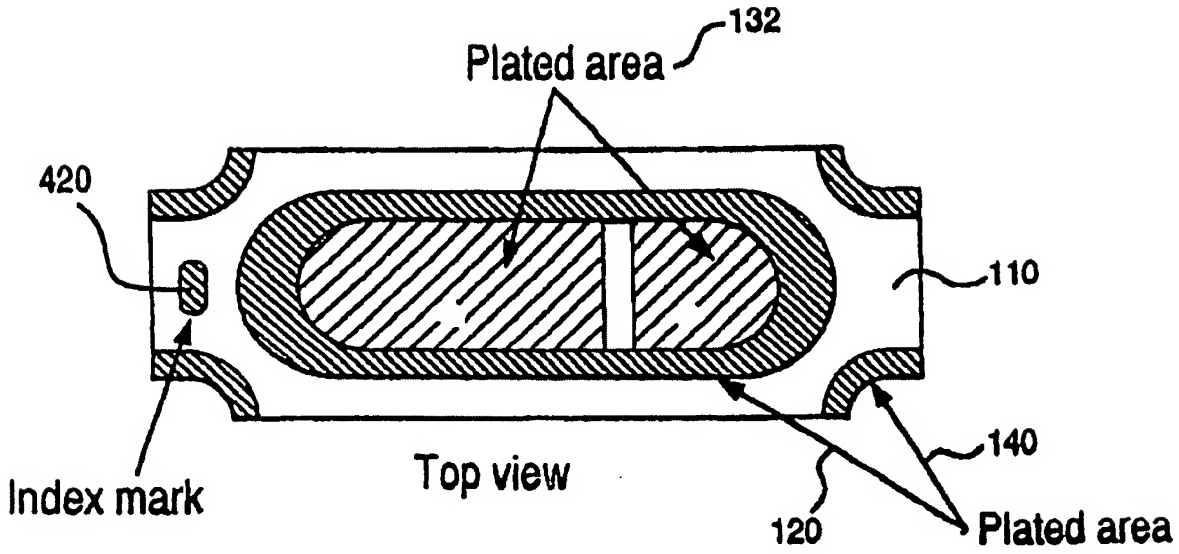


Fig. 4 of the present application

Fig. 2D set forth above shows optically transparent material 145 disposed in the cavity in which light emitting diode 130 is located, and substantially vertical sidewalls 110 being contiguous and continuous with the substrate at the intersections thereof. Fig. 2D also shows that the housing comprising the substrate and the substantially vertical sidewalls 110 is formed form a single unitary piece of ceramic. Fig. 4 set forth above shows plated area 120 disposed on portions of substrate 110 for reflecting light from an LED in a predetermined direction.

The independent claims of the present application are claims 1 and 8, which are reproduced hereinbelow as currently pending in a format showing where specific support for each element recited therein may be found in the specification and drawings as originally filed (see page and line numbers shown in italicized square brackets set forth after each element). It should be noted that support for elements recited in claims 1 and 8, in addition to that shown below, may be found throughout the specification, drawings and abstract of the present application.

1. (previously presented) A standalone light emitting diode package *[Figs. 1 and 4, package 100/110]* comprising:

a housing comprising substantially vertical sidewalls and a substrate *[Figs. 1 and 4, see elements 110; page 7, lines 3-5; page 8, lines 2 and 3 and 7-10; page 9, line 21 and page 10, lines 11-2; page 10, lines 5-8; page 11, lines 13-18]*, the sidewalls and the substrate defining a cavity having a bottom *[Fig. 1; page 3, lines 3 and 12; page 6, line 12]*, the substrate being located at the bottom of the cavity *[Fig. 1; page 3, lines 3 and 12; page 6, line 12]*, the substrate and the vertical sidewalls being contiguous, continuous and uninterrupted respecting one another at the

intersections thereof, the housing forming a single unitary piece of ceramic *[Figs. 1 and 4, see elements 110; Figs. 2C and 2D, element 110, where sidewalls and substrate are contiguous, continuous and uninterrupted respecting one another; page 9, lines 20-24, where a ceramic package is described as being formed using a die that can be stamped on a sheet of ceramic material to form the LED package 110; step 302 in Fig. 3 and corresponding description on page 10, lines 3-8]*;

at least one light-reflective metallic coating disposed over at least portions of the sidewalls and the substrate *[Figs. 1 and 4, see element 120; page 6, lines 21-24; page 7, lines 7-9; page 8, lines 12-19; page 10, lines 1421; page 10, line 23 through page 11, line 5; page 12, lines 21-23]*;

a light emitting diode mounted on or in the substrate *[Fig. 1, see element 130; page 7, lines 14-17; page 11, lines 9-18; page 11, lines 20-22]*, and

an optically transparent material disposed in the cavity and covering the light emitting diode *[Fig. 2D, see element 145; Fig. 3, step 308; page 12, lines 8-17]*;

wherein the ceramic composition and configuration of the housing and the light-reflective coating cooperate to minimize light leakage through, into or out of the housing when the light emitting diode is energized *[page 3, lines 6 and 7; page 6, lines 18-24; page 7, lines 7-13; page 7, lines 21224 and page 8, line 1; page 13, lines 12-23]*, the metallic coating reflects light incident thereon in a predetermined direction *[page 3, lines 7-9; page 8, lines 21-22; page 11, lines 2-5]*, and the optically transparent material protects the light emitting diode *[page 12, lines 8-17]*.

8. (previously presented) A method of making a standalone light emitting diode package *[Figs. 1, 3 and 4, package 100/110; page 9, lines 20-24 and page 10, lines 8]*, the package comprising a housing having substantially vertical sidewalls and a substrate *[Figs. 1 and 4, see elements 110; page 7, lines 3-5; page 8, lines 2 and 3 and 7-10; page 9, line 21 and page 10, lines 11-2; page 10, lines 5-8; page 11, lines 13-18]*, the sidewalls and the substrate defining a cavity having a bottom *[Fig. 1; page 3, lines 3 and 12; page 6, line 12]*, the substrate being located at the bottom of the cavity *[Fig. 1; page 3, lines 3 and 12; page 6, line 12]*, the substrate and the vertical sidewalls being contiguous, continuous and uninterrupted respecting one another at the intersections thereof, the housing forming a single unitary piece of ceramic *[Figs. 1 and 4, see elements 110; Figs. 2C and 2D , element 110, where sidewalls and substrate are contiguous, continuous and uninterrupted respecting one another; page 9, lines 20-24, where a ceramic package is described as being formed using a die that can be stamped on a sheet of ceramic material to form the LED package 110; step 302 in Fig. 3 and corresponding description on page 10, lines 3-8]*, at least one light-reflective metallic coating being disposed over at least portions of the sidewalls and the substrate *[Figs. 1 and 4, see element 120; page 6, lines 21-24; page 7, lines 7-9; page 8, lines 12-19; page 10, lines 14-21; page 10, line 23 through page 11, line 5; page 12, lines 21-23]*, a light emitting diode being mounted on or in the substrate *[Fig. 1, see element 130; page 7, lines 14-17; page 11, lines 9-18; page 11, lines 20-22]*, an optically transparent material being disposed in

the cavity and covering the light emitting diode *[Fig. 2D, see element 145; Fig. 3, step 308; page 12, lines 8-17]*, the ceramic composition and configuration of the housing and the light-reflective coating cooperating to minimize light leakage through, into or out of the housing when the light emitting diode is energized *[page 3, lines 6 and 7; page 6, lines 18-24; page 7, lines 7-13; page 7, lines 21224 and page 8, line 1; page 13, lines 12-23]*, the metallic coating reflecting light incident thereon in a predetermined direction *[page 3, lines 7-9; page 8, lines 21-22; page 11, lines 2-5]*, and the optically transparent material protecting the light emitting diode *[page 12, lines 8-17]*, the method comprising:

(a) stamping the housing from the single unitary piece of ceramic *[Figs. 1 and 4, see elements 110; Figs. 2C and 2D , element 110, where sidewalls and substrate are contiguous, continuous and uninterrupted respecting one another; page 9, lines 20-24, where a ceramic package is described as being formed using a die that can be stamped on a sheet of ceramic material to form the LED package 110; step 302 in Fig. 3 and corresponding description on page 10, lines 3-8]*;

(b) coating the at least portions of the sidewalls and substrate with the at least one light-reflective metallic coating *[Fig. 3, step 304; Figs. 1 and 4, see element 120; page 6, lines 21-24; page 7, lines 7-9; page 8, lines 12-19; page 10, lines 14-21; page*

10, line 23 through page 11, line 5; page 12, lines 21-23];

(c) mounting the light emitting diode on or in the substrate *[Fig. 3, step 306; Fig. 1, see element 130; page 7, lines 14-17; page 11, lines 9-18; page 11, lines 20-22]*, and

(d) depositing the optically transparent material in the cavity *[Fig. 3, step 308; Fig. 1, see element 130; page 7, lines 14-17; page 11, lines 9-18; page 11, lines 20-22; Fig. 2D, see element 145; Fig. 3, step 308; page 12, lines 8-17]*.

VI. Grounds of Rejection to Be Reviewed on Appeal

In the Final Office Action mailed July 6, 2007 the Examiner rejected all of now pending claims 1 and 3-14 on the basis of two U.S. patents and one Japanese patent. The particular grounds of rejection to be reviewed on appeal are as follows:

(1) Whether claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 are obvious under 35 U.S.C. 103(a) over U.S. Patent No. 6, 355, 946 to Ishinaga (hereafter "the Ishinaga reference") in view of Japanese Patent No. 2002232017 to Kyocera (hereafter "the Kyocera reference") and U.S. Patent No. 5,686,790 to Curtin et al. (hereafter "the Curtin reference");

(2) Whether claims 4 and 10 are obvious under 35 U.S.C. 103(a) over the Ishinaga reference in view of the Kyocera reference and the Curtin reference and further in view of U.S. Patent No. 6,186,649 to Zou (hereafter "the Zou reference");

(3) Whether claims 7 and 13 are obvious under 35 U.S.C. 103(a) over the Ishinaga reference in view of the Kyocera reference and the Curtin reference and further in view of U.S. Patent No. 6,715,901 to Huang (hereafter "the Huang reference");

VII. Arguments

A. The Examiner's Arguments

In regards to: (1) claims 1, 3, 5, 6, 8, 9, 11, 12 and 14; (2) claims 4 and 10; and (3) claims 7 and 13, the Examiner stated, respectively:

(1) **With respect to claims 1, 3, 5, 6, 8, 9, 11, 12 and 14:**

In the Final Office Action (and as substantially repeated in the Examiner's Answer), the Examiner stated:

> Claims 1, 3, 5-6, 8-9, 11-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga (U.S. Patent 6,355,946) in view of Kyocera (JP 2002232017) and Curtin et al. (U.S. Patent 5,686,790).
>
> Regarding claim 1, Ishinaga discloses a standalone light emitting diode package (abstract) comprising a housing comprising sidewalls (Fig. 1) and a substrate (reference number 1), the sidewalls and the substrate defining a cavity having a bottom (Fig. 1, see bottom portion of dotted lines), the substrate being located at the bottom of the cavity (Fig. 1, reference number 1), portions of the substrate engaging or being adjacent to the sidewalls (Fig. 2, see elliptical dotted line in the middle), die substrate being formed of ceramic (column 3, lines 50-55), at least one light-reflective metallic coating disposed over at least portions of the substrate (column 3, lines 65-68), a light emitting diode mounted on or in the substrate (abstract, Fig. 1), and optically transparent material disposed in the cavity and covering the light emitting diode (column 4, lines 25-30), wherein the ceramic composition of the substrate and the composition of the sidewalls and the light-reflective coating cooperate to minimize light leakage through or into the housing when the light emitting diode is energized (column 4, lines 55-65), the metallic coating reflects light incident thereon in a

predetermined direction (column 3, lines 65-68, and Fig. 1), and the optically transparent material protects the light emitting diode (column 4, lines 25-30). Ishinaga does not disclose the metallic coating on the sidewalls and the vertical sidewalls being formed of one continuous and unitary piece of ceramic.

Kyocera discloses substantially vertical sidewalls (Fig. 4, reference number 33), the substantially vertical sidewalls being formed of ceramic (English abstract), and at least one light-reflective metallic coating disposed over at least portions of the sidewalls (Fig. 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the configuration of Kyocera in the apparatus of Ishinaga to make the apparatus produce more light. See the English abstract of Kyocera.

Curtin et al. discloses substantially vertical sidewalls (Fig. 7), the vertical sidewalls being contiguous, continuous and uninterrupted respecting one another at the intersections thereof (Fig. 7, reference number 701), the housing forming a single unitary piece of ceramic (reference number 701, Fig. 7), the housing minimizing light leakage through, into or out of the housing (Fig. 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the configuration of Curtin et al. in the apparatus of Ishinaga to enable one to attach driver circuits to the substrate (column 3, line 55, to column 4, line 6, of Curtin et al.).

Regarding claims 3 and 9, Ishinaga discloses the cavity being substantially white in color (column 4, lines 30-35).

Concerning claims 5 and 11, Ishinaga discloses the metallic coating comprising gold (column 3, lines 65-68, Fig. 1).

Regarding claims 6 and 12, Ishinaga discloses the metallic coating being formed by plating (column 3, lines 65-68).

Regarding claim 8, Ishinaga discloses a housing having sidewalls (Fig. 1) and a substrate (reference number 1), the sidewalls and the substrate defining a cavity having a bottom (Fig. 3, lower middle), the substrate being located at the bottom of the cavity (Fig. 1), portions of the substrate engaging or being adjacent to the sidewalls (Fig. 1), the substrate being formed of ceramic (column 3, lines 50-55), at least one light-reflective metallic coating being disposed over at least portions of the substrate (column 3, lines 65-68, Fig. 1), a light emitting diode being mounted on or in the substrate (abstract, Fig. 1, reference number 3A), an optically transparent material being disposed in the cavity and covering the light emitting diode (column 4, lines 25-30), the ceramic composition of the substrate and the composition of the sidewalls and the light-reflective coating cooperating to minimize light leakage through or into the housing when the light emitting diode is energized (column 4, lines 55-65), the metallic coating reflecting light incident thereon in a predetermined direction (column 3, lines 65-68, and Fig. 1), and the optically transparent material protecting the light emitting diode (column 4, lines 25-30), the method comprising providing the housing (Fig. 1), coating at least portions of the substrate with a light-reflective metallic coating (column 3, lines 65-68), mounting the light emitting diode on or in the substrate (Fig. 1, abstract) and depositing the optically transparent material in the cavity (column 4, lines 25-30). Ishinaga does not disclose stamping the ceramic, the substantially vertical sidewalls being unitary with each other or with a metallic coating, or the step of coating the sidewalls with the at least one light-reflective metallic coating.

Kyocera discloses substantially vertical sidewalls (Fig. 4, reference number 33), the substantially vertical sidewalls being formed of ceramic (English abstract), at least one light-reflective metallic coating disposed over at least portions of the sidewalls (Fig. 4), and the step of coating the at least portions of the sidewalls with the at least one light-reflective metallic coating (Fig. 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the configuration of Kyocera in the apparatus of Ishinaga to make the apparatus produce more light. See the English abstract of Kyocera.

Curtin et al. discloses substantially vertical sidewalls (Fig. 7), the vertical sidewalls being contiguous, continuous and uninterrupted respecting one another at the intersections thereof (Fig. 7, reference number 701), the housing forming a single unitary piece of ceramic (reference number 701, Fig. 7), the housing minimizing light leakage through, into or out of the housing (Fig. 7), and the step of stamping the housing from the single unitary piece of ceramic (column 24, lines 10-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the configuration of Curtin et al. in the apparatus of Ishinaga to enable one to attach driver circuits to the substrate (column 3, line 55, to column 4, line 6, of Curtin et al.).

Concerning claim 14, Ishinaga discloses the step of depositing epoxy as the optically transparent material in the cavity (column 4, lines 25-30).

In the Answer, the Examiner further stated:

Appellant argues that claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 are not obvious over Ishinaga in view of Kyocera and Curtin (page 39, Appellant's Brief of 10/4/07). More specifically, Appellant argues that none of the cited references show the following: "a *housing comprising substantially vertical sidewalls and a substrate formed form* [sic] a *single unitary piece of ceramic[;]* * * * *at least one light-reflective metallic coating disposed over at least portions of the sidewalls and the substrate[\]* * * * *a housing forming a single unitary piece of ceramic* [;]* * * a *ceramic composition and configuration of a housing and a tight-reflective coating that cooperate to minimize light leakage through or into the housing when a light emitting diode is energized.* (Page 44, Appellant's Brief dated 10/4/07, emphasis in the original.)

To the contrary, these elements are shown in the combination of Ishinaga, Kyocera and Curtin. The housing with vertical sidewalls is disclosed by Ishinaga (see Fig. 3 on the right and left reprinted by the Appellant on page 23 of the Appellants Brief of 10/4/07). The light reflective metallic coating disposed over at least portions of the sidewalls is admitted by Appellant on page 24 of the Appeal Brief dated 10/4/07. Ishinaga discloses the conductive traces on the base (column 3, lines 65-68). (The portions of the base with the conductive traces is a portion of the base with a metallic coating, because the conductive traces also reflect light; even a small portion of a metallic coating is a metallic coating that reflects light.) Nothing in the claim requires that the metallic coating cover most of the base. Furthermore, nothing teaches against substantially vertical sidewalls in Kyocera. Drawing 4 may be designated as prior art and not as advantageous as the invention ultimately described in Kyocera. However, a reference is not teaching against something just because it says that it is disadvantageous or otherwise not as good as the invention featured in the document. A reference must specifically teach one reading the reference that some certain thing should not be done, not that something is just not as good. See MPEP 2123 and 2145 (X)(D) (1).

The housing forming a single unitary piece of ceramic is disclosed in Curtin on Fig. 7 as reprinted by the Appellant on page 32 of the Appeal Brief dated 10/4/07. Appellant contends that the fact that the ceramic is in layers means that the structure is not unitary. To the contrary, nothing in the definition of unitary means that the base and sidewalls have to be solid ceramic. One of the definitions of the word "unitary" states as follows: "based on or characterized by unity or units" *(Merriam-Webster's Collegiate Dictionary,* Tenth Edition, page 1288). The layers are laminated and formed to make a unit as shown in Fig. 7 of Curtin. Thus, the element of the claim is met and the rejections should be upheld.

As to the last point, Ishinaga discloses the housing and coating cooperating to minimize light leakage in Fig. 3 as reproduced by Appellant on page 23 of the Appeal Brief dated 10/4/07. Any structure cooperates to minimize light leakage just by blocking some of the light. Nothing in the claim specifies how much light leakage is prevented or gives any figures on the efficiency of the apparatus. Therefore, this element of the claim is met. Thus, it is respectfully submitted that the rejections should be upheld.

Appellant goes to a lot of trouble to say that the references should not be combined because no teaching or suggestion exists in the references themselves to make the combination. To the contrary *KSR v. Teleflex* indicates that the Teaching, Suggestion, Motivation Test is just one of many tests for motivation that can be used (82 USPQ2d 1385, 1396 (US 2007)). Furthermore, most of the motivations stated in the rejections come from the references themselves or the English abstracts of the references, which means that they meet the Teaching, Suggestion, Motivation Test. The motivation to use Huang comes from knowledge available to one of ordinary skill in the art, which is also allowed by *KSR v. Teleflex*. *Id.*

Since the motivations disclosed in the rejections meet the standards put forth by *KSR v. Teleflex*, the Appellant cannot say that impermissible hindsight reasoning is present. It must also be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the Appellant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this case the motivations only take into account knowledge available to a person of ordinary skill in the art, and the combinations should be considered permissible.

Regarding Appellant's argument on page 48 of the Appeal Brief dated 10/4/07 about the economic infeasibility of the combination of the cited references is not pertinent to the determination of whether or not the claims are allowable. See MPEP 2145 (VII). Thus, this argument is irrelevant and should not be considered.

(2) **With respect to claims 4 and 10:**

In the Final Office Action (and as substantially repeated in the Examiner's Answer), the Examiner stated:

> Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga in view of Kyocera and Curtin et al. as applied to claims 1 and 8 above, and further in view of Zou et al. (U.S. Patent 6,186,649).
>
> Concerning claims 4 and 10, Ishinaga, Kyocera and Curtin et al. do not disclose using silver as a reflective coating. Zou et al. discloses the metallic coating comprising silver (column 6, lines 10-15).
>
> It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the silver coating of Zou et al. in the apparatus of Ishinaga, Kyocera and Curtin et al. to achieve "high output irradiance[.]" See column 1, lines 60-65, of Zou et al.

In the Answer, the Examiner further stated:

> The arguments concerning Zou et al. and Huang stand or fall with the arguments above, which are not accepted for the reasons delineated above. Thus, it is respectfully submitted that the rejections using these references should be upheld as well.

(3) **With respect to claims 7 and 13:**

In the Final Office Action (and as substantially repeated in the Examiner's Answer), the Examiner stated:

> Claims 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga in view of Kyocera and Curtin et al. as applied to claims 1 and 8 above, and further in view of Huang (U.S. Patent 6,715,901).
>
> Regarding claims 7 and 13, Ishinaga, Kyocera and Curtin et al. do not disclose the cavity being formed (or configured) to contain a plurality of LEDs. Huang discloses the ceramic cavity being formed to contain a plurality of LEDs (column 4, lines 62-67).
>
> It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the configuration of Huang in the apparatus of Ishinaga, Kyocera and Curtin et al. to increase light output per apparatus.
>
> Applicant's arguments with respect to claims 1 and 3-14 have been considered but are moot in view of the new ground(s) of rejection.

In the Answer, the Examiner further stated:

> The arguments concerning Zou et al. and Huang stand or fall with the arguments above, which are not accepted for the reasons delineated above. Thus, it is respectfully submitted that the rejections using these references should be upheld as well.

The foregoing rejections and comments made by the Examiner are responded to in detail below.

B. The Cited References

(1) The Ishinaga Reference

The first reference relied upon is the Ishinaga reference (U.S. Patent No. 6,355,946), which discloses a semiconductor device with a reflector. The semiconductor device includes a substrate, a semiconductor chip for emitting light, and a reflector enclosing the semiconductor chip for reflecting the light emitted from the semiconductor chip. The substrate is provided with a first electrode and a second electrode each electrically connected with the semiconductor chip. A transverse cross-section of the reflector defines an elongated figure, such as oblong, elliptical, rhombic or rectangular. See the Abstract of the Ishinaga reference.

Reference to Fig. 3 of the Ishinaga reference, reproduced hereinbelow, and portions of the specification corresponding thereto (*e.g.*, columns 3 and 4 thereof), shows that substrate 1A is formed separately from casing 5, and that casing 5 is formed of a different material (a polycarbonate resin) than is substrate 1A (formed from a polyimide resin or ceramic). Ishinaga discloses inner-wall surface 5a as being parabolic or curved in shape such that the amount of space available at the base of casing 5 for the mounting of a light source on substrate 1A is limited. No reflective coating is disposed over portions of substrate 1A of Ishinaga.

FIG.3

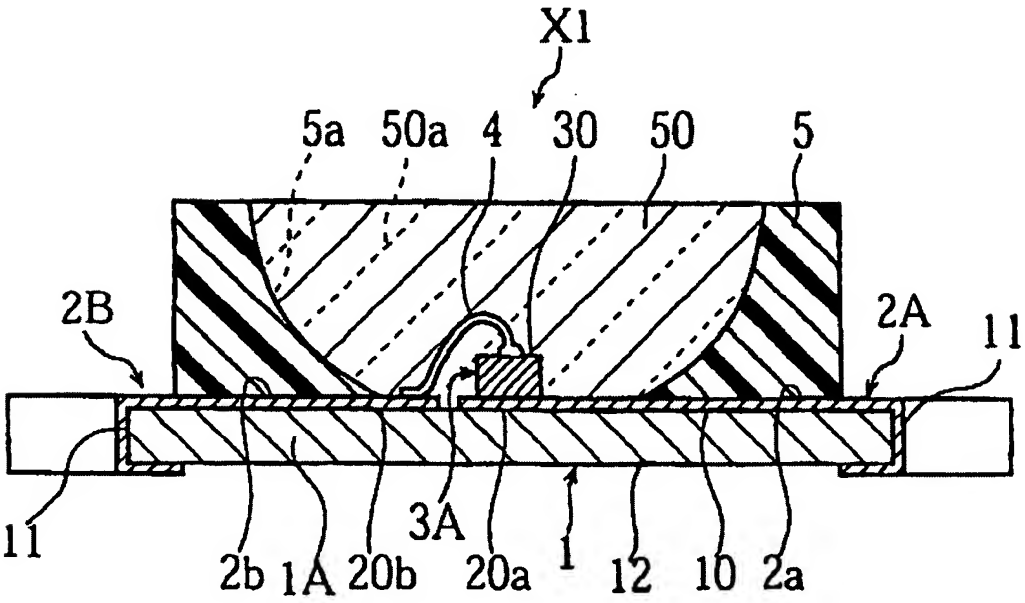


Fig. 3 of the Ishinaga reference

(2) The Kyocera Reference

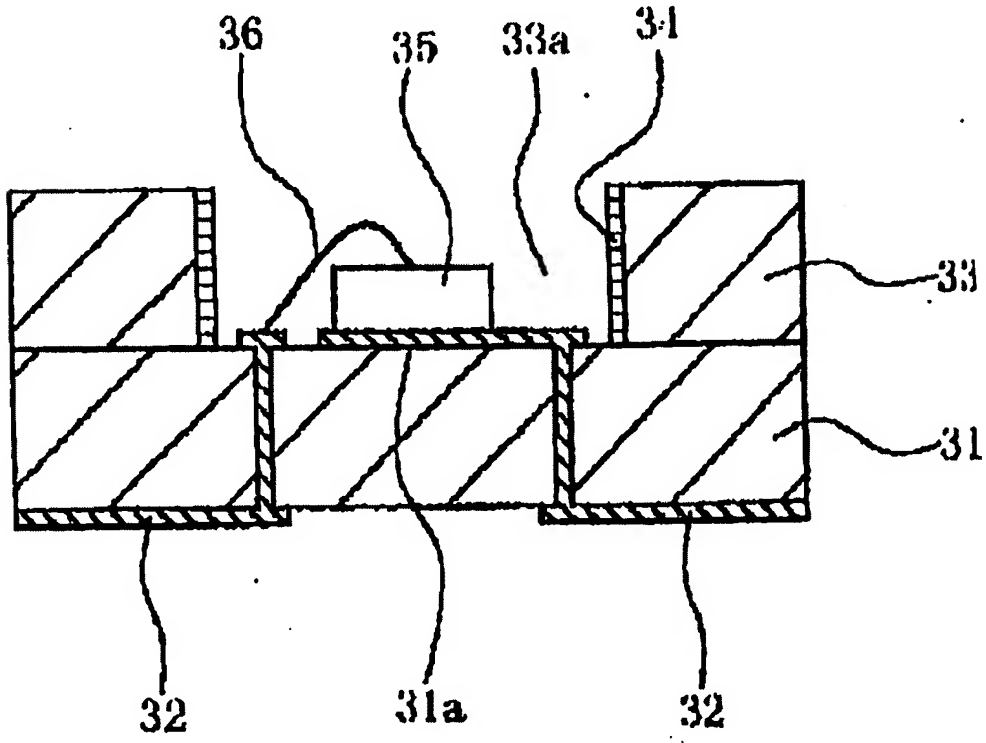
The second reference relied upon is the Kyocera reference (Japanese Patent No. 2002-232017), which discloses a package for storing a light emitting element and method of making same.

A machine translation of the complete Kyocera reference from the Japanese Patent Office website (the original of which is in Japanese) reveals that this reference discloses at least two different embodiments of a ceramic lighting package. Drawing 4 of the Kyocera reference shows a first such embodiment (see below), where ceramic sash 33 has vertical sidewalls and is mounted on flat ceramic base 31. Conductors/vias 32 are disposed through ceramic base 31 to provide electrical power to light emitting device 35. The Kyocera reference further discloses filling sash 33 with a "transparent closure resin" and forming such a package from separate pieces of metallized ceramic having pre-formed conductors and holes, as appropriate, formed therein.

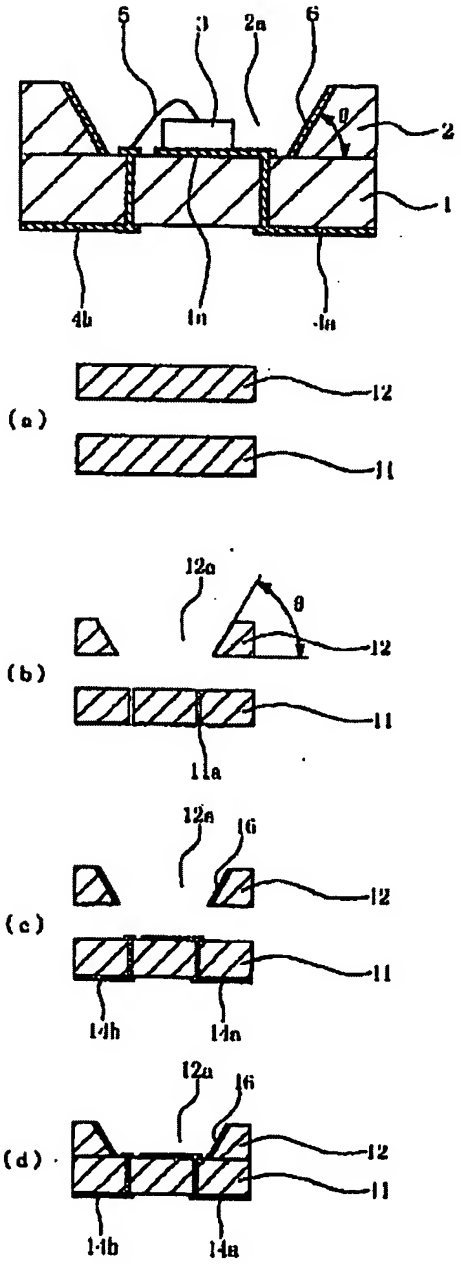
The lighting package embodiment shown in Drawing 4 is discussed in the context of representing prior art, and as such is noted as having poor "luminous efficiency" and poor lighting "homogeneity" respecting a second embodiment of a lighting package illustrated in Drawings 1 through 3 of the Kyocera reference (see below), where a ceramic sash 2 is disclosed as having metallized sidewalls 6 having an angle between 55 and 70 degrees respecting horizontal base 1. Such angled or slanted sidewalls 6 are disclosed as providing "superior luminous efficiency" with "uniform and efficient" distribution of the light emitted by light emitting element

3. Like the first embodiment, the second embodiment disclosed in the Kyocera reference features a ceramic base 1 formed separate and apart from sash 2, and conductors 4a and 4b formed within and through ceramic base 1 for powering light emitting device 3.

Nowhere does the Kyocera reference appear to mention anything regarding heat transfer or conductivity of a lighting package, problems associated with designing a thermally efficient lighting package, any or differences in the thermal conductivity of the first and second embodiments disclosed therein.



Drawing 4 of the Kyocera Reference



Drawings 1-3 of the Kyocera Reference

(3) The Curtin Reference

The third reference relied upon is the Curtin reference (U.S. Patent No. 5,686,790), which discloses a flat panel device with a ceramic backplate. The flat panel device includes a faceplate, a backplate made of a co-fired ceramic substrate and attached to the faceplate to form a sealed enclosure, and a structure for producing light. The faceplate includes an active region. The light producing structure is divided into a matrix of "display elements," or a plurality of "light producing elements." Driver circuitry is formed on or attached to a surface of the backplate. The driver circuitry is connected to the display elements or light producing elements by electrically conductive vias formed entirely or partially through or within the ceramic substrate, and electrically conductive traces formed within or on one or more surfaces of the ceramic substrate. Each of the display elements or light producing elements is controlled by the driver circuitry to cause light emission at a corresponding pixel or pixels of the faceplate active region. See the Abstract of the Curtin reference.

Pertinent portions of the Curtin reference include the following:

> This invention relates to the use of a ceramic substrate as the backplate of a flat panel device such as a flat panel display. More particularly, this invention relates to the use of a co-fired ceramic substrate-- and, most particularly, ***a multilayer co-fired ceramic substrate*** -- as the backplate of a flat panel device. *Col. 1, lines 21-26 of U.S. Patent No. 5,686,790 to Curtin et al.*

Electrically conductive traces and regions are formed on layers of ***multilayer ceramic substrates*** according to the invention using low cost conventional thick film patterning. High resolution (lines and spaces on the order of less than 2 mils wide) of features on the ceramic substrate according to the invention can be achieved. Vias in ceramic substrates according to the invention are formed using low cost, high tolerance via hole forming techniques such as laser drilling, gang punching or direct infusion. *Col. 5, lines 20-29 of U.S. Patent No. 5,686,790 to Curtin et al.*

One example of a low temperature ceramic material which can be used for the purposes of this invention is DuPont's Green Tape (trademark of DuPont). This material, available in thin sheets (e.g., approximately 3 to 10 mils) has a relatively low firing temperature, about 900.degree. to 1000.degree. C., and includes plasticizers in the unfired state which provide excellent workability. The Green Tape product is a mixture of ceramic particles and amorphous glass, also in particulate form, with binders and plasticizers. See U.S. Pat. Nos. 4,820,661, 4,867,935, and 4,948,759. The material in the unfired form is adaptable to deposition of conductive metal traces, such as by screen printing or other techniques.

Other materials having the desired properties in the unfired state, such as devitrifying glass tape, ceramic tape or ceramic glass tape material, and possibly amorphous glass in a flexible matrix, are also adaptable for the purposes of the invention; the term "ceramic" is used generally herein to refer to this class of materials. Broadly speaking, the requirements of such a material are that ***(a) it be producible in thin layers***, (b) the layers be flexible in the unfired state, ***(c) holes can be put in a layer or several layers together in the unfired state, (d) the holes can be filled with conductors where desired,*** (e)

conductive traces can be put accurately on the surfaces of the unfired layers, (f) the layers can be laminated, in that they are bonded together at least on a final firing, (g) the fired structure have a coefficient of thermal expansion that can be substantially matched to that of a face plate and a back plate of preferred materials such as float glass, ***(h) the fired, laminated structure be rigid and strong,*** (i) the fired structure be vacuum compatible, (j) the fired structure not contain materials which will poison cathodes, and (k) all materials and fabrication be possible at practical cost. *Col. 7, lines 20-40 of U.S. Patent No. 5,686,790 to Curtin et al.*

Backplate 201 is a co-fired ceramic substrate. In the embodiment shown in FIG. 2A, ***backplate 201 includes two layers 201a and 201b. However, any desired number of layers can be used, i.e., one, three or more layers.*** Currently, ceramic substrates having up to 60 layers, e.g., IBM ES9000 module, have been commercially produced. *Col. 8, lines 15-19 of U.S. Patent No. 5,686,790 to Curtin et al.*

According to the invention, the ceramic substrate is a co-fired substrate, i.e., both the ceramic layer or layers and the material that forms the electrically conductive traces and regions on the ceramic layer or layers and fills vias in the ceramic layer or layers are fired at the same time. ***The ceramic substrate according to the invention includes one or more thin (0.3-15 mil) ceramic layers. The ceramic substrate can include any number of layers; as many as 60 layers have been used in commercially available ceramic substrates*** (e.g., IBM ES9000 module). More typically, the ceramic substrate includes 5-10 layers. *Col. 11, lines 50-60 of U.S. Patent No. 5,686,790 to Curtin et al.*

As shown by block 303, the sheets of ceramic tape are then laminated to form ***a multilayer substrate***, and, as shown by block 304, fired to fuse the sheets of ceramic tape together to form an integral, rigid, vacuum compatible substrate. Within, the multilayer substrate, the vias formed in each sheet combine to form through-hole, blind and semi-blind vias that serve as electrical interconnects between metallization, e.g., electrically conductive traces, formed on different layers of the ceramic substrate. ***The use of a multilayer ceramic substrate with metallization on each layer and vias interconnecting metallization on different layers*** enables the effective conductor density (i.e., the equivalent conductor density on a single layer) to be greatly increased since, theoretically, the effective conductor density can be made as large as the conductor density on a single layer multiplied by the number of layers. *Col. 12, lines 42-57 of U.S. Patent No. 5,686,790 to Curtin et al.*

[Referring to Fig. 7] Backplate 701 is a co-fired ceramic substrate that can be formed with any of the materials and processes described above. In order to create the step change between interior surfaces 701b and 701f, a rectangular hole is formed, by for instance, stamping, in one or more of the ceramic layers of the backplate 701 ***before the ceramic layers are laminated together.*** The wall portions 701a of backplate 701 can be formed from ceramic layers in the same manner ***(i.e., stamping an appropriately sized hole in the ceramic layers before lamination) and laminated and fired together with the remainder of backplate 701 to form an integral structure.*** The wall portions 701a

are attached to faceplate 702 with frit glass 710 to form sealed enclosure 703. Alternatively, the wall portions 701a can be formed separately from backplate 701 (as in FIGS. 2A and 2B above) and attached to both faceplate 702 and backplate 701 with, for example, frit glass. *Col. 24, lines 9-24 of U.S. Patent No. 5,686,790 to Curtin et al.*

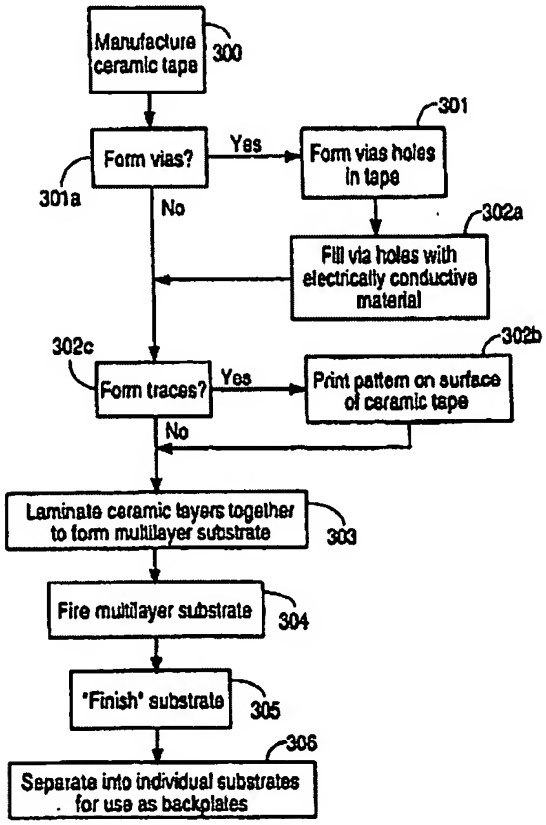


FIG. 3

Fig. 3 of the Curtin Reference

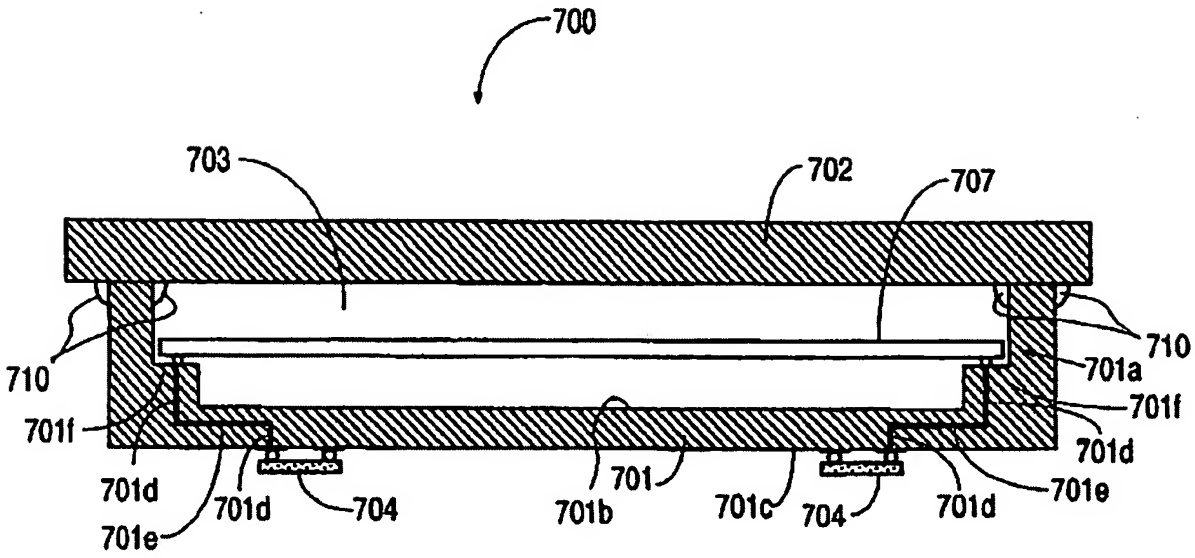


FIG. 7

Fig. 7 of the Curtin Reference

(4) The Zou Reference

The fourth reference relied upon is the Zou reference (U.S. Patent No. 6,186,649), which discloses a linear illumination source that utilizes external, highly reflective enclosures containing one or more linear openings to achieve improved source efficiency, output irradiance and/or output radiance. Such illumination sources may be combined with additional optical elements to produce more complex illumination systems. See the Abstract of the Zou reference.

Pertinent portions of the Zou reference include the following:

> Diffuse reflectors can be made that have very high reflectivities (for example, greater than 95% or greater than 98%). However, diffuse reflectors with high reflectivities are generally quite thick. For example, diffuse reflectors with reflectivities greater than 98% are typically several millimeters thick. Examples of diffuse reflectors include, but are not limited to, fluoropolymer materials such as Spectralon.TM. from Labsphere, Inc. and polytetrafluoroethylene) film from Fluorglas (sold under the trade name Furon.TM.), W. L. Gore and Associates, Inc. (sold under the trade name DR.TM.), or E. I. du Pont de Nemours & Company (sold under the trade name of Teflon.TM.), films of barium sulfate, porous polymer films containing tiny air channels such as polyethersulfone and polypropylene filter materials made by Pall Gelman Sciences, and polymer composites utilizing reflective filler materials such as, for example, titanium dioxide. An example of the latter material is titanium-dioxide-filled ABS (acrylonitrile-butadiene-styrene terpolymer) produced by RTP. In the case that a structural material is employed as a reflective material, such as titanium dioxide filled ABS, the structural support 104 can be combined with the reflective layer 106 as shown in FIGS. 4 and 5.

Most specular reflective materials have reflectivities ranging from about 80% to about 93%. Any light that is not reflected by the specular reflector is absorbed and converted to heat, thus lowering the efficiency of any optical system utilizing such a reflector. Examples of specular reflective materials include, but are not limited to, Silverlux.TM., a product of 3M, and other carrier films of plastic which have been coated with a thin metallic layer such as silver, aluminum or gold. The thickness of the metallic coating may range from about 0.05 .mu.m to about 0.1 mm, depending on the materials used and the method of manufacturing the metal coating. *Col. 5, line 51 through col. 6, line 16 of U.S. Patent No. 6,186,649 to Zou et al.*

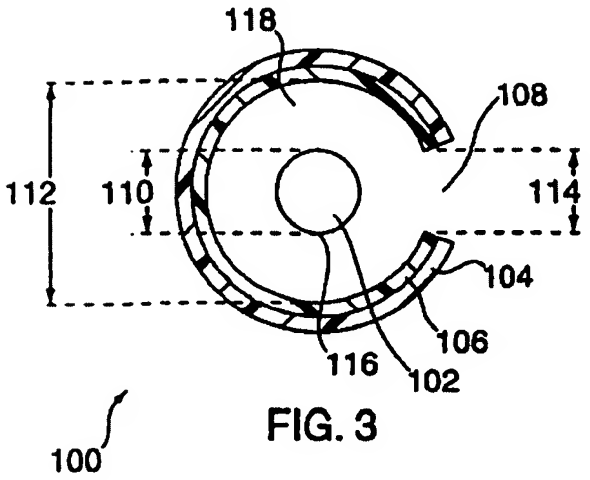


FIG. 3

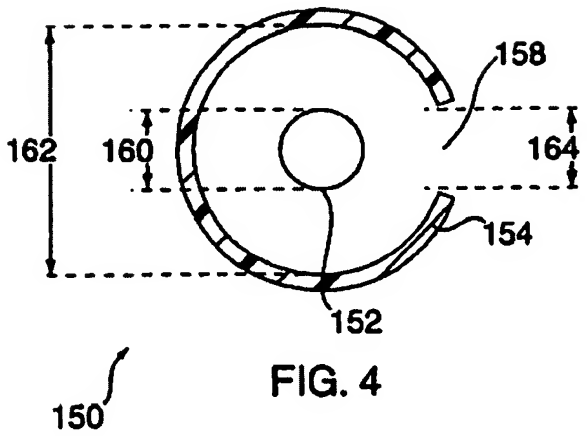


FIG. 4

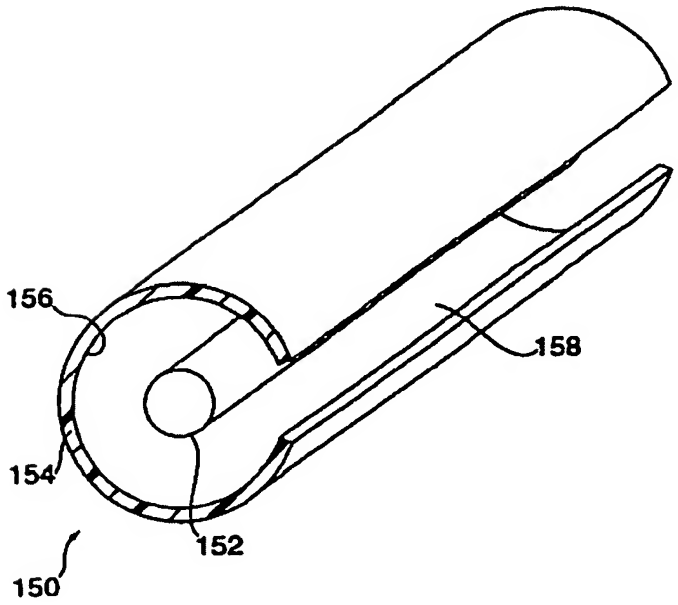


FIG. 5

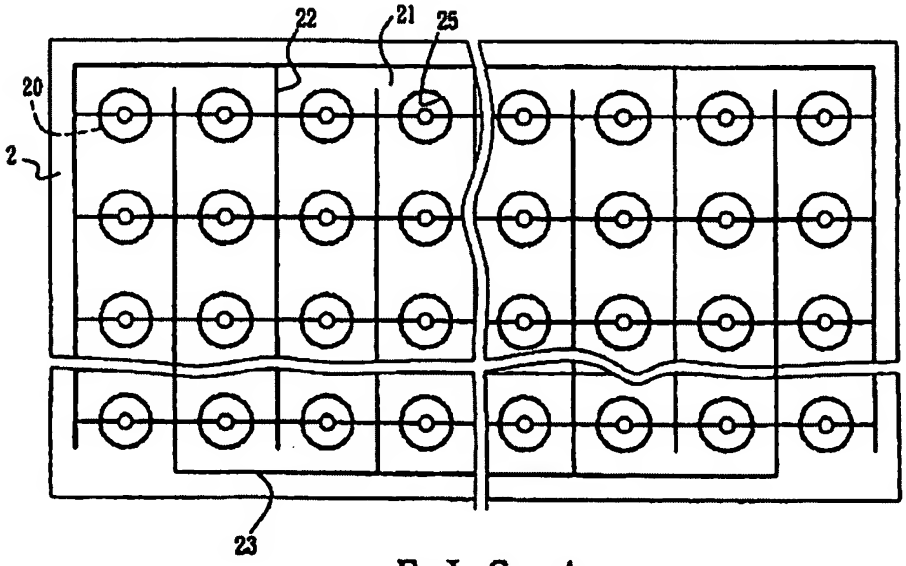
Figs. 3, 4 and 5 of the Zou Reference

(5) The Huang Reference

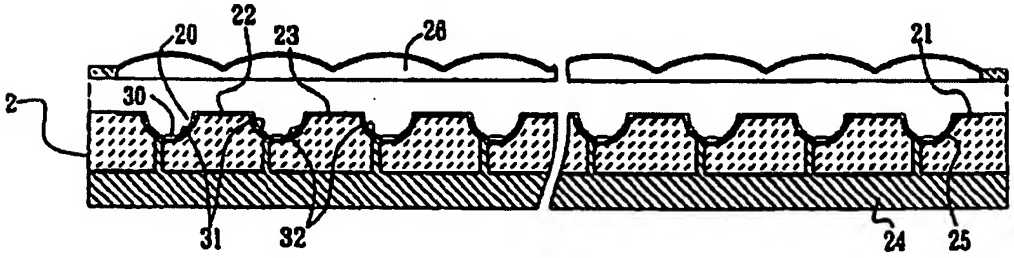
The fifth reference relied upon is the Huang reference (U.S. Patent No. 6,715,901), which discloses an image projector system including a light source, a light-modulating device, and a projector lens set. The light source includes a rectangular housing formed with a light-transmissive output port and at least four light-transmissive input ports, at least four light emitting diode modules, and a mirror set mounted in the housing for directing light beam outputs of the light emitting diode modules that are transmitted into the housing through the light-transmissive input ports to pass through the light-transmissive output port for processing by the light-modulating device. The light beam output of each of the light emitting diode modules has a wavelength band within a range of from 400 to 700 nanometers, that is different from the other light emitting diode modules and that has a center wavelength spaced apart from that of the other light emitting diode modules by at least 20 nanometers. See the Abstract of the Huang reference.

Pertinent portions of the Zou reference include the following:

Each of the light emitting diode modules 12, 13, 14, 15 includes a plurality of light emitting diodes, the light beams generated by the diodes in the same one of the light emitting diode modules 12, 13, 14, 15 having a substantially uniform wavelength band. As shown in FIGS. 4 and 5, each light emitting diode module includes a ceramic substrate 2 having a front side 21 and a rear side. The front side 21 is formed with an array of diode receiving cavities 20. Each of the cavities 20 is formed with a reflective layer 25 for increasing the light emitting efficiency. The rear side is formed with a plurality of holes that extend respectively toward the reflective layers 25 in the cavities 20. Each light emitting diode module further includes an array of light emitting semiconductor diodes 30, each of which is mounted on and is insulated from the reflective layer 25 of a respective one of the cavities 20 in the front side 21 of the substrate. Each of the semiconductor diodes 30 has first and second diode terminals 31, 32. The front side 21 of the substrate 2 is formed with a first circuit 22, in the form of conductive fingers, connected to the first diode terminals 31 of the semiconductor diodes 30, and a second circuit 23, also in the form of conductive fingers that are interleaved with the conductive fingers of the first circuit 22, connected to the second diode terminals 32 of the semiconductor diodes 30. To prevent overheating of the semiconductor diodes 30, in this embodiment, a metal heat dissipating member 24 is mounted on the rear side of the substrate 2 and extends into the holes in the substrate 2 to establish thermal conduction with the reflective layers 25 in the cavities 21. An active cooling apparatus, such as a cooling pipe (not shown), may be disposed under the heat dissipating member 24 to enhance the cooling effect, thereby effectively lowering the temperature of the working environment of the semiconductor diodes 30.



F I G. 4



F I G. 5

Fig. 4 and 5 of the Huang Reference

C. Applicant's Arguments

(1) Claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 are not obvious over the Ishinaga reference in view of the Kyocera reference and the Curtin reference.

Despite the Examiner's repeated assertions to the contrary, reference to claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 will show that those claims contain limitations disclosed nowhere in the cited Ishinaga, Kyocera and Curtin references. More particularly, reference to claim 1 is instructive, as it contains limitations similar to those found in all the other claims that yet remain pending in the present application. With further reference to Figs. 2D and 4 of the present application, claim 1 recites the following:

(a) A standalone light emitting diode package, comprising:

(b) a housing comprising substantially vertical sidewalls and a substrate;

(c) the sidewalls and the substrate defining a cavity having a bottom, the substrate being located at the bottom of the cavity, the substrate and the vertical sidewalls being contiguous and continuous with one another at the intersections thereof;

(d) the housing forming a single unitary piece of ceramic;

(e) at least one light-reflective metallic coating disposed over at least portions of the sidewalls and the substrate;

(f) a light emitting diode mounted on or in the substrate, and

(g) an optically transparent material disposed in the cavity and covering the light emitting diode;

(h) wherein the ceramic composition and configuration of the housing and the light-reflective coating cooperate to minimize light leakage through, into or out of the housing when the light emitting diode is energized;

(i) the metallic coating reflects light incident thereon in a predetermined direction, and

(j) the optically transparent material protects the light emitting diode.

Each of claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 requires all of elements (a) through (j) set forth above, or their substantial equivalents.

Referring first to the Ishinaga reference, it becomes clear that Ishinaga et al. disclose none of elements (a), (c), (d), (e), (g), (h), (i) or (j) set forth above, or their respective equivalents, recited in claims 1, 3, 5, 6, 8, 9, 11, 12 and 14. The Ishinaga reference and corresponding portions of the specification thereof show that substrate 1A is formed separately from casing 5, and that casing 5 is formed of a different material (a polycarbonate resin) than is substrate 1A (formed from a polyimide resin or ceramic). Ishinaga discloses inner-

wall surface 5a as being parabolic or curved in shape such that the amount of space available at the base of casing 5 for the mounting of a light source on substrate 1A is limited. No reflective coating is disposed over portions of substrate 1A of Ishinaga. There is no discussion in the Ishinaga reference regarding the thermal conductivity attributes or characteristics of ceramic lighting packages, or of light leaktightness being compromised by seams or gaps disposed between separate package components.

In the Answer dated December 31, 2007, the Examiner asserts that the Ishinaga reference discloses some of the elements pointed out hereinabove as not being disclosed in the Ishinaga reference. For example, at page 7 of the Examiner's Answer it is asserted that the Ishinaga reference discloses "vertical sidewalls," thereby meeting claim limitation (b) shown above. Reference to Fig. 3 of the Ishinaga reference cited by the Examiner as disclosing such "vertical sidewalls," however, shows that the vertical sidewalls in question are the ***exterior sidewalls*** of the device disclosed by Ishinaga, not the "substantially vertical sidewalls" recited in the present claims, which owing to their inter-relationship with other elements recited in the claims can only be interior sidewalls.

On page 8 of the Examiner's Answer it is asserted that the Appeal Brief filed October 4 "admits" a "metallic coating" being disclosed in the Ishinaga reference. This assertion is untrue. Reference to page 24 of the Appeal Brief cited by the Examiner shows that no such admission is made in respect of the Ishinaga reference.

On page 8 of the Examiner's Answer it is asserted that Ishinaga's conductive traces (elements 2A and 2B in Fig. 3) "also reflect light" and therefore meet the limitations of element (e) shown above ("at least one light-reflective metallic coating disposed over at least portions of the sidewalls and the substrate"). Reference to Fig. 3 and the newly cited portions of the text of the Ishinaga reference (*i.e.*, col. 3, lines 65-68) shows first that most of conductors 2a and 2b are covered by casing 5 and thus unavailable to reflect light, second that no portion of those conductors is disposed on sidewalls or inner wall surface 5a (which is required by element (e)), and third that Ishinaga et al. clearly have no intention of providing a light reflectivity function with conductors 2a and 2b. The Examiner goes on to state that "nothing in the claim requires that the metallic coating cover most of the base." While assertion may be true, it ignores the fact that element (e) requires that the metallic coating be "disposed over at least portions of the sidewalls ***and*** the substrate." Thus, the assertion that element (e) in the present claims is met by the disclosure of Ishinaga is simply not true.

Referring now to the Kyocera reference, it becomes clear that the Kyocera reference discloses none of elements (c), (d), (e) or (h) set forth above, or their respective equivalents, recited in claims 1, 3, 5, 6, 8, 9, 11, 12 and 14. Instead, and as described in detail above, Drawing 4 of the Kyocera reference and corresponding portions of the specification thereof show that that no light-reflective coating is disposed over the bottom surface of cavity 33a. Instead, Kyocera's Fig. 4 shows electrically conductive strip 31a disposed at the bottom of cavity 33a and connected to LED 35. Vias and electrical conductors 32 route electrical power to LED 35 through substrate 31 and clearly serve no light-reflecting function whatsoever. Sidewalls 33 and substrate 31 are not contiguous, continuous and uninterrupted respecting

one another at the intersections thereof because the housing comprising such sidewalls and substrate is not formed from a single unitary piece of ceramic, and instead is formed from multiple laminae which are subsequently joined together. As described in detail above, the Kyocera reference teaches away from a ceramic lighting package having substantially vertical sidewalls by stating that such an embodiment is disadvantageous and has undesirable optical illumination properties. Finally, there is no discussion in the Kyocera reference regarding the thermal conductivity attributes or characteristics of ceramic lighting packages, or of light leaktightness being compromised by seams or gaps disposed between separate ceramic components.

On page 8 of the Examiner's Answer it is asserted that "nothing teaches against substantially vertical sidewalls in Kyocera." This statement is not true. The Kyocera reference explicitly states that the device with vertical sidewalls illustrated in Fig. 4 thereof exhibits undesirable light homogeneity and efficiency characteristics. See paragraph [0007] of the Kyocera reference English translation provided in the Examiner's Answer as an answer thereto.

Moreover, the Kyocera reference explicitly states that it is directed towards overcoming the problems presented by the prior art vertical sidewall device of Fig. 4 by providing devices having sloping sidewalls. In other words, the Kyocera reference presents a classic example of teaching away from a claimed invention. One of ordinary skill in the art reading the Kyocera reference would be motivated to use sloping sidewalls, not the problem-causing vertical sidewalls of the prior art.

The burden to be met in showing that the Kyocera reference teaches away from the presently claimed invention is not that articulated by the Examiner in the Answer. There is no requirement in the case law requiring that an affirmative, explicit statement be made that a thing must not be done to constitute teaching away. Rather, it is a "clear discouragement" of the teaching in question. Here, Kyocera explicitly states that the vertical sidewall device of Fig. 4 has undesirable characteristics and those undesirable characteristics are eliminated by replacing vertical sidewalls with sloping sidewalls. If such a statement in the Kyocera reference does not rise to the level of "clear discouragement," then the legal standard for teaching away is meaningless.

Referring next to the Curtin reference, it becomes clear that the Curtin reference discloses none of elements (a), (c), (d), (e), (g), (h) or (i) set forth above, or their respective equivalents, recited in claims 1, 3, 5, 6, 8, 9, 11, 12 and 14. Indeed, the Curtin reference pertains to providing ceramic flat panel devices for CRTs ("cathode ray tubes"), and discloses nothing respecting light emitting diode packages.

As described in detail above, Fig. 3 and numerous other portions of the Curtin reference show that Curtin et al. disclose forming a flat panel CRT display from multiple layers of co-fired ceramic. Contrary to the Examiner's assertions, Curtin et al. do not disclose forming a housing from a single unitary piece of ceramic (purportedly shown in Fig. 7 at reference number 701), stamping the housing from a single unitary piece of ceramic (purportedly disclosed at col. 24, lines 10-15), or providing a housing that minimizes light leakage therethrough (purportedly disclosed in Fig. 7). Instead, even a brief perusal of the portions of the Curtin reference cited by the Examiner in support of the proposition that various elements recited in

the present claims are disclosed in the Curtin reference shows that such portions of the Curtin reference do not, in fact, disclose the purported elements.

For example, Fig. 7 shows that conductive traces 701e and vias 701d are disposed through and within ceramic backplate 701. Numerous portions of the specification of the Curtin reference disclose forming backplate from multiple co-fired layers of ceramic and forming conductive traces thereon and vias therethrough before the layers are joined together and formed. Indeed, it would be impossible to form traces 701e, which are internal to backplate 701, by any method other than by forming same atop one layer and placing another layer thereover. Thus, backplate 701 in Fig. 7 must be formed from multiple layers of ceramic. Moreover, such a multi-layer structure is entirely consistent with the disclosure of the Curtin reference. Moreover. the Curtin reference specifically states that stamping a hole in a ceramic layer may be carried out ***before the ceramic layers are laminated together*** (see col. 24, lines 1015), and thus does not disclose "stamping the housing from a single unitary piece of ceramic." Finally, as in the Ishinaga and Kyocera references, there is no discussion in the Curtin reference regarding the thermal conductivity attributes or characteristics of ceramic lighting packages, or of light leaktightness being compromised by seams or gaps disposed between separate package components.

On page 8 of the Examiner's Answer it is asserted that "[a] housing forming a single unitary piece of ceramic is disclosed in Curtin on Fig. 7," "nothing in the definition of unitary means that the base and sidewalls have to be solid ceramic" and "[t]he layers are laminated and formed to make a unit as shown in Fig. 7 of Curtin" (apparently in reference to the presently-pending claims). These statements are not true. First and as discussed in detail above, the Curtin reference discloses ***only*** layers of ceramic being

laminated together to form a housing. See Fig. 7 of the Curtin reference. Second, the patent law clearly permits the applicant to be his own lexicographer. The meaning of element (d) shown above and appearing in all the presently-pending claims (namely, "the housing forming a single unitary piece of ceramic") could not be any more apparent in the light of the plain language employed therein and the voluminous file history of the present patent application and clearly ***does not mean*** a housing comprising multiple layers that have been laminated together. Moreover, the Examiner conveniently ignores the word "single" appearing in element (d) before the terms "unitary piece of ceramic." Single means one, not a plurality, as would clearly be required to arrive at a housing structure comprising multiple layers of ceramic. Thus, element (d) is clearly not met by the Curtin reference.

Reference to the various elements of claim 1 as presented above will show that this claim, and all other claims yet pending in the present application, contain ***many limitations disclosed nowhere*** in the cited Ishinaga, Kyocera and Curtin references.

More particularly, reference to the claim 1 as presented hereinabove shows that elements (c) [the sidewalls and the substrate defining a cavity having a bottom, the substrate being located at the bottom of the cavity, the substrate and the vertical sidewalls being contiguous, continuous and uninterrupted respecting one another at the intersections thereof], (d) [the housing forming a single unitary piece of ceramic], and (e) [at least one light-reflective metallic coating disposed over at least portions of the sidewalls and the substrate], and (h) [wherein the ceramic composition and configuration of the housing and the light-reflective coating cooperate to minimize light leakage through or into the housing when the light emitting diode is energized] are simply not disclosed, described, hinted at or suggested anywhere in the Ishinaga, Kyocera or Curtin references, either

alone or in combination. In other words, at least four separate but inter-related structural elements recited in the still-pending claims are missing from the cited references.

Thus, none of the three cited references ***discloses a housing comprising substantially vertical sidewalls and a substrate formed form a single unitary piece of ceramic.***

None of the three cited references ***discloses at least one light-reflective metallic coating disposed over at least portions of the sidewalls and the substrate.***

None of the three cited references ***discloses a housing forming a single unitary piece of ceramic.***

And none of the three cited references ***discloses a ceramic composition and configuration of a housing and a light-reflective coating that cooperate to minimize light leakage through or into the housing when a light emitting diode is energized.***

The Applicants have discovered that a certain novel combination of structural, ceramic and electronic elements combined in a certain order and arranged in a certain manner are required to produce the beneficial effects of the present invention. Those elements and arrangements are neither disclosed nor suggested anywhere in the Ishinaga, Kyocera or Curtin references, and accordingly cannot be *prima facie* obvious.

On page 9 of the Examiner's Answer, short shrift is given to the idea that a motivation or suggestion must appear somewhere in the prior art to properly combine elements found in disparate references. As in the Final Office Action, no such motivation or suggestion is provided by the Examiner for combining disparate elements from the cited references, other than the mere assertion that they should be combined because one of ordinary skill in the art would be motivated to combine such references (without saying

why) and therefore the claimed invention is obvious (again without saying why).

There is no incentive, teaching or suggestion in the Ishinaga or Kyocera references to produce the invention now recited in claims 1, 3, 5, 6, 8, 9, 11, 12 and 14. The mere fact that the cited Ishinaga, Kyocera and Curtin references could, with the benefit of hindsight, produce something vaguely similar to the present invention does not make the modification obvious, or suggest the desirability of the modification required to arrive at the present invention. Indeed, this conclusion is buttressed by the fact that numerous elements and limitations are missing in the Ishinaga, Curtin and Kyocera references in respect of claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 set forth herein (namely, elements (c), (d), (e) and (h) contained in all of claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 as enumerated above).

It is well settled that a motivation to combine elements or limitations disclosed in disparate references *must be found within the references themselves or from pertinent sources of information,* and that such a motivation does not arise, as here, by merely identifying a collection of disparate piece parts in different references, and then asserting it would have been obvious to take such disparate elements and limitations and add many others thereto to arrive at the presently claimed invention.

In such a context, and as pointed out above, it is particularly noteworthy that the cited Ishinaga, Curtin and Kyocera references ***disclose nothing concerning some of the problems solved by the present invention***, such as facilitating the high-speed and economic manufacture of ceramic housings for LED packages by stamping housing sidewalls and a substrate from a single unitary piece of ceramic, reducing light leakage from an LED package, increasing the brightness of light emitted by an LED package, permitting LED packages of equivalent brightness to be made

smaller, decreasing power requirements for an LED package, permitting a greater number of multiple LEDs to be mounted in an LED package than would otherwise be possible, and permitting manufacturing of an LED package to be carried out at high temperatures.

There is no suggestion of what direction any experimentation should follow in the Ishinaga, Curtin and Kyocera references to obtain the invention recited in claims1, 3, 5, 6, 8, 9, 11, 12 and 14. Accordingly, the result effective variables, for example providing a ceramic housing formed from a single unitary piece of ceramic and disposing a reflective coating over at least portions of the substantially vertical sidewalls and the substrate thereof, are not known to be result effective. Thousands or millions of attempts at variations might be made before arriving at the desired improvement. Thus, to say that it is obvious to read the Ishinaga, Curtin and Kyocera references and somehow arrive at the invention now recited in claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 is clearly not the test for obviousness.

The foregoing analysis also makes it clear that there is no basis in the art for modifying the teachings of the Ishinaga, Curtin and Kyocera references to arrive at the invention now recited in claims 1, 3, 5, 6, 8, 9, 11, 12 and 14. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some reason, teaching, suggestion or incentive supporting the combination. As pointed out in detail above, the Ishinaga and Kyocera references do not teach the problems associated with, or the sources of such problems, respecting facilitating the high-speed and economic manufacture of ceramic housings for LED packages by stamping housing sidewalls and a substrate from a single unitary piece of ceramic, reducing light leakage from an LED package, increasing the brightness of light emitted by an LED package,

permitting LED packages of equivalent brightness to be made smaller, decreasing power requirements for an LED package, permitting a greater number of multiple LEDs to be mounted in an LED package than would otherwise be possible, and permitting manufacturing of an LED package to be carried out at high temperatures.

When, as here, the prior art itself provides no apparent reason for one of ordinary skill in the art to make a modification or to combine references, an argument clearly does not exist that the claimed subject matter is obvious. Thus, using the applicants' own disclosure as a blueprint to reconstruct in hindsight the invention recited in claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 out of isolated teachings appearing in the prior art is clearly improper.

The results and advantages produced by the invention set forth in claims 1, 3, 5, 6, 8, 9, 11, 12 and 14, and of which the cited Ishinaga, Curtin and Kyocera references are utterly devoid, cannot be ignored simply because the claim limitations might be deemed similar to the otherwise barren prior art.

The foregoing analysis also makes it clear that many limitations appearing in claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 are simply not present in the Ishinaga, Curtin and Kyocera references. When evaluating a claim for determining obviousness, ***all limitations of the claim must be evaluated.*** Under §103, claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 cannot be dissected in turn, the various individual elements recited in the claims excised, and then the remaining portions of the mutilated claims declared to be unpatentable. The basic rule of claim interpretation of reading the claims as a whole must be followed. Accordingly, the Ishinaga, Curtin and Kyocera references may not properly be used as a basis for rejecting claims 1, 3, 5, 6, 8, 9, 11, 12 and 14 under §103.

The functions, ways and results provided by the devices and methods disclosed in the Ishinaga, Curtin and Kyocera references are completely different from those provided by the presently claimed invention. The LED packages disclosed in the Ishinaga and Kyocera references function to emit light without reflecting light from reflective coatings disposed on the substrates thereof, and employ multiple ceramic components to form an LED package housing. The flat panel CRT devices of Curtin are configured to provide a CRT display of minimal thickness having a backplate upon which electronic components such as ASICS or other chips may be mounted. In respect of the many problems solved by the present invention, the results provided by Ishinaga, Curtin and Kyocera are identical: the structures disclosed in all three references, or the structures that might somehow be produced by combining the elements disclosed in the three references, are ***incapable of preventing or reducing light leakage from the LED packages thereof in respect of prior art devices, and are much more difficult, expensive and time-consuming to manufacture.***

Note that the Examiner's comments appearing at the bottom of page 9 and the top of page 10 of the Answer regarding the "economic infeasibility" of prior art devices being "not pertinent to the determination of whether or not the claims are allowable" ignores decades of jurisprudence that have developed since *John Deere v. Graham* concerning indicia of nonobviousness. Such indicia include commercial success, long felt but unresolved needs, the failure of others, and recognition of a problem. All these factors relate in one way or another to the advantages of the presently-claimed invention, including its commercial advantages.

Finally, there is no combination of disparate elements from the Ishinaga, Curtin and Kyocera references that could possibly result in the present invention. Instead, and in a light most favorable to the mythical person of ordinary skill in the art, combining elements from those three references might result in an LED package having a housing formed from separate components (e.g., a substrate having separate sidewalls mounted thereon), a substrate having no reflective coating disposed thereon, and an LED package exhibiting no decreased light leakage in respect of prior art devices.

For all the foregoing reasons and more, the presently claimed invention is not *prima facie* obvious in view of the Ishinaga, Curtin and Kyocera references, alone or in combination.

(2) **Claims 4 and 10 are not obvious over the Ishinaga reference in view of the Kyocera, Curtin and Zou references.**

Reference to the portions of the Zou patent cited by the Examiner shows that there is no disclosure of information that adds anything substantive to the deficiencies of the Ishinaga, Curtin and Kyocera references described and analyzed in detail above. Indeed, the referenced portions of the Zou patent merely state, respectively, "a highly-efficient, linear illumination source with high output irradiance and radiance from a narrow opening is needed" and "[e]xamples of specular reflective materials include, but are not limited to, Silverlux, a product of 3M, and other carrier films of plastic which have been coated with a thin layer such as silver, aluminum or gold." Col. 1, lines 60-65 and col. 6, lines 10-15 of the Zou patent.

Accordingly, and in view of the many limitations missing from the Ishinaga, Curtin, Kyocera and Zou references, alone or in combination, and the completely barren nature of such references respecting the many problems solved by the presently-claimed invention (*e.g.*, improving heat transfer and reducing LED package temperatures, reducing light leakage from an LED package or forming a housing from a single, unitary piece of ceramic), claims 4 and 10 cannot be prima facie obvious over or in view of any combination of such references.

(3) **Claims 7 and 13 are not obvious over the Ishinaga reference in view of the Kyocera, Curtin and Huang references.**

Reference to the portions of the Huang patent cited by the Examiner shows that there is no disclosure of information that adds anything substantive to the deficiencies of the Ishinaga, Curtin and Kyocera references described and analyzed in detail above. Indeed, the referenced portions of the Huang patent state "[e]ach of the light emitting diode modules 12, 13, 14 and 15 includes a plurality of light emitting diodes, the light beams generated by the diodes in the same of the light emitting diode modules 12, 13, 14, 15 having a substantially uniform wavelength band." Col. 4, lines 62-67 of the Huang patent.

Accordingly, and in view of the many limitations missing from the Ishinaga, Curtin, Kyocera and Huang references, alone or in combination, and the completely barren nature of such references respecting the many problems solved by the presently-claimed invention (*e.g.*, improving heat transfer and reducing LED package temperatures, reducing light leakage from an LED package, and forming a housing from a single unitary piece of ceramic), claims 7 and 13 cannot be prima facie obvious over or in view of any combination of such references.

VIII. Summary

The rejections of claims 1 and 3-14 will now be seen to rest fundamentally upon an argument that missing elements not present in the cited references would somehow be provided by one of ordinary skill in the art. No explanation is given as to where the missing elements would be found or developed, or why they would be provided. Moreover, and in addition to at least four different elements recited in the presently-pending claims not being disclosed in the cited references, nowhere has the Examiner pointed to a single factually-based motivation for combining the cited references other than the conclusory statement that one of ordinary skill would be motivated to do so. Accordingly, the arguments articulated by the Examiner do not establish a *prima facie* case of obviousness respecting the presently-pending claims. The advantages and beneficial results provided by the presently-claimed invention are numerous, and merit patentability.

Claims 1 and 3-14 remain pending in the present application, and are believed to be in condition for allowance. Review and allowance of the claims as presented herein is requested. The Board is respectfully requested to contact the undersigned by telephone or e-mail with any questions or comments they may have.

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Claims Appendix

1. A standalone light emitting diode package, comprising:

a housing comprising substantially vertical sidewalls and a substrate, the sidewalls and the substrate defining a cavity having a bottom, the substrate being located at the bottom of the cavity, the substrate and the vertical sidewalls being contiguous, continuous and uninterrupted respecting one another at the intersections thereof, the housing forming a single unitary piece of ceramic;

at least one light-reflective metallic coating disposed over at least portions of the sidewalls and the substrate;

a light emitting diode mounted on or in the substrate, and an optically transparent material disposed in the cavity and covering the light emitting diode;

wherein the ceramic composition and configuration of the housing and the light-reflective coating cooperate to minimize light leakage through, into or out of the housing when the light emitting diode is energized, the metallic coating reflects light incident thereon in a predetermined direction, and the optically transparent material protects the light emitting diode.

3. The light emitting diode package of Claim 1 wherein said cavity is substantially white in color.

4. The light emitting diode package of Claim 1 wherein said metallic coating comprises silver.

5. The light emitting diode package of Claim 1 wherein said metallic coating comprises gold.

6. The light emitting diode package of Claim 1 wherein said metallic coating is formed by plating.

7. The light emitting diode package of Claim 1 wherein said cavity is formed to contain a plurality of light emitting diodes.

8. A method of making a standalone light emitting diode package, the package comprising a housing having substantially vertical sidewalls and a substrate, the sidewalls and the substrate defining a cavity having a bottom, the substrate being located at the bottom of the cavity, the substrate and the vertical sidewalls being contiguous, continuous and uninterrupted respecting one another at the intersections thereof, the housing forming a single unitary piece of ceramic, at least one light-reflective metallic coating being disposed over at least portions of the sidewalls and the substrate, a light emitting diode being mounted on or in the substrate, an optically transparent material being disposed in the cavity and covering the light emitting diode, the ceramic composition and configuration of the housing and the light-reflective coating cooperating to minimize light leakage through, into or out of the housing when the light emitting diode is

energized, the metallic coating reflecting light incident thereon in a predetermined direction, and the optically transparent material protecting the light emitting diode, the method comprising:

(a) stamping the housing from the single unitary piece of ceramic;

(b) coating the at least portions of the sidewalls and substrate with the at least one light-reflective metallic coating;

(c) mounting the light emitting diode on or in the substrate, and

(d) depositing the optically transparent material in the cavity.

9. The method as described in Claim 8 wherein said cavity is substantially white in color.

10. The method as described in Claim 8 wherein said light reflective material comprises silver.

11. The method as described in Claim 8 wherein said light reflective material comprises gold.

12. The method as described in Claim 8 wherein said reflective coating is formed using plating.

13. The method as described in Claim 8 wherein said cavity is configured to mount a plurality of light emitting diodes therein.

14. The method as described in Claim 8 further comprising depositing epoxy as the optically transparent material in the cavity.

Evidence Appendix

None.

Related Proceedings Appendix

None.